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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER

PAPPAS, PETER

ART UNIT PAPER NUMBER

2628

DATE MAILED: 04/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/790,953

Applicant(s)

SEILER ET AL.

Examiner

Peter-Anthony Pappas

Art Unit

2671

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 11 October 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-25 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-25 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 02 March 2004 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, a hierarchical Z buffer and stencil cache updater must be shown or the feature(s) canceled from the claim(s). It is noted a hierarchical update and kill/pass module 178 is illustrated in Fig. 4. No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

2. Claims 22-24 are objected to because of the following informalities: There are duplicate claims numbered 22. For the purposes of art rejection the second claim 22 is considered claim 23, claim 23 is considered 24 and claim 24 is considered claim 25. In addition their respective dependencies are considered to change accordingly.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aila et al. (U.S. Pub. No. US 2005/0134588 A1) in view of Greene et al. (U.S. Patent No. 5, 579, 455).

5. In regards to claim 1 Aila et al. teaches a method and apparatus for image processing (Abstract; p. 2, ¶ 18). When images are processed, the frame buffer (including the color buffer and the z buffer) containing pixels of an image is typically divided into sets of pixels often called tiles. The tiles are often non-overlapping rectangular areas. For example, an image can be divided into non-overlapping 8x8 pixel regions (p. 3-4, ¶ 52).

To accelerate rendering of an image, the following extra information is often stored for each tile: the minimum of all depth values in the tile, Zmin, and the maximum

of all depth values in the tile, Z_{max} . It is appreciated that for processing shadow information more efficiently, a new concept may be introduced. The perimeter of the tile and the minimum and maximum depth values define a tile volume. For a rectangular tile, for example, the tile volume is a 3D axis-aligned box in screen space, defined by the horizontal and vertical bounds of the rectangular tile together with the Z_{min} and Z_{max} values (p. 4, ¶ 53).

It is appreciated that the tile volume need not necessarily be defined using the minimum and maximum depth values relating to a tile. A tile volume can be determined using the depth values relating to a tile in a different way. An alternative is, for example, the use of two planes: one plane in front of all depth values relating to a tile, and the other plane behind the depth values, for instance. The planes can be determined based on the depth values relating to the tile. The Z_{min} and Z_{max} values are, however, a very convenient way to define the tile volume, as this information is typically available (p. 4, ¶ 53).

To further enhance the performance of the graphics processor, it is possible to use a hierarchical stencil buffer or other hierarchical information store for shadow information (stencil code). If the result (stencil value) of the stencil test can be determined from a tile-specific entry of the hierarchical stencil buffer (containing a shadow mask), the per-pixel stencil buffer entries need not be accessed (p. 6, ¶ 83; p. 7, ¶ 88; Fig. 4).

Aila et al. fails to explicitly teach a hierarchical Z value range. Greene et al. teaches a hierarchical Z-buffer scan-conversion algorithm that does well on both (a)

quickly rejecting most of the hidden geometry in a mode, and (b) exploiting the spatial and temporal coherence of the images being generated. The method uses two hierarchical data structures, an object-space octree and an image-space Z-pyramid, in order to accelerate scan conversion. The two hierarchical data structures make it possible to reject hidden geometry (hierarchical Z value test fails) very rapidly while rendering visible geometry (hierarchical Z value test passes) with the speed of scan conversion (Abstract).

It would have been obvious to one skilled in the art, at the time of the applicant's invention, to incorporate the teachings of Greene et al. into the method taught by Aila et al., because through such incorporation the rejection of hidden geometry, through the use of depth information, would be improved in terms of speed, thus allowing for more information to be processed in a shorter amount of time.

6. In regards to claim 2: stencil test fails see Aila et al., p. 7, ¶ 86; stencil test passes see Aila et al., p. 7, ¶ 89; and hierarchical Z value test passes (Greene et al., Abstract).

7. In regards to claim 3 the rationale disclosed in the rejection of claim 2 is incorporated herein.

8. In regards to claim 4: stencil test fails see Aila et al.: p. 7, ¶ 86.

9. In regards to claim 5 see Greene et al., column 11, lines 4-12; column 15, lines 48-67; column 16, lines 1-6; column 17, lines 24-40.

10. In regards to claim 6 see Aila et al., p. 9, ¶ 102, 106.

11. In regards to claim 7 the rationale disclosed in the rejection of claim 1 is incorporated herein. It is noted each of said depth elements 512 are considered to represent respective pixel elements 204 (Fig. 2, 5A) and therefor results, at least in part, in per-pixel processing.

12. In regards to claim 8 the rationale disclosed in the rejection of claim 1 is incorporated herein.

13. In regards to claim 9 Aila et al. teaches that if the Boolean boundary value (indicator) in the temporary tile classification buffer is TRUE for a tile, this needs to be rasterized using a finer resolution, for example, using per-pixel resolution. Otherwise the rasterization can be skipped, because the entire tile is either in shadow or lit (p. 7, ¶ 86).

14. In regards to claim 10 the rationale disclosed in the rejection of claim 7 is incorporated herein.

15. In regards to claim 11 the rationale disclosed in the rejection of claim 8 is incorporated herein (Aila et al., p. 6, ¶ 83; p. 7, ¶ 88; Fig. 8).

16. In regards to claim 12 the rationale disclosed in the rejection of claim 6 is incorporated herein.

17. In regards to claim 13 Greene et al. further teaches that if the Z-pyramid value is closer, we know the primitive is hidden in the quadrant. If we fail to prove that the primitive is hidden in one of the quadrants, we go to the next finer level of the pyramid for that quadrant and try again. Ultimately, we either prove that the entire polygon is hidden, or we recurse down to the finest level of the pyramid and find a pixel covered by

the polygon that has a Z-value farther away than the nearest Z value in the polygon (column 6, lines 28-36). The rationale and motivation disclosed in the rejection of claim 5 is incorporated herein.

18. In regards to claim 14 the rationale disclosed in the rejection of claim 8 is incorporated herein. It is noted that when respective pixels of a tile are considered lit, respective to a mask, and a hierarchical Z value test passes that a positive indication is considered to be set.

19. In regards to claim 15 the rationale disclosed in the rejection of claims 3 and 4 are incorporated herein.

20. In regards to claim 16 the rationale disclosed in the rejection of claim 8 is incorporated herein.

21. In regards to claim 17 the rationale disclosed in the rejection of claims 1 and 5 is incorporated herein. It is noted a comparator (Aila et al., Fig. 5, element 501) is considered coupled to a hierarchical Z buffer (Aila et al., Fig. 5, element 521; Greene et al., Fig. 1, element 104), stencil cache (Aila et al., Fig. 5, element 523) and hierarchical Z buffer and stencil cache updater (Aila et al., Fig. 5m, element 510).

22. In regards to claim 18 the rationale disclosed in the rejection of claim 17 is incorporated herein.

23. In regards to claim 19 the rationale disclosed in the rejection of claim 17 is incorporated herein.

24. In regards to claim 20 the rationale disclosed in the rejection of claim 14 is incorporated herein.

25. In regards to claim 21 the rationale disclosed in the rejection of claim 4 is incorporated herein. Aila et al. teaches a tile processing and classifying module 513 (kill) module which is coupled to said hierarchical Z buffer and stencil cache updater.

26. In regards to claim 22 it is noted that data stored in said buffers is either ignored or retrieved (updated) based on said indicator.

27. In regards to claim 23 the rationale disclosed in the rejection of claim 17 is incorporated herein.

28. In regards to claim 24 the rationale disclosed in the rejection of claim 17 is incorporated herein.

29. In regards to claim 25 the rationale disclosed in the rejection of claim 22 is incorporated herein.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Peter-Anthony Pappas whose telephone number is 571-272-7646. The examiner can normally be reached on M-F 9:00am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ulka Chauhan can be reached on 571-272-7782. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Peter-Anthony Pappas
Examiner
Art Unit 2628

PAP


ULKA CHAUHAN
SUPERVISORY PATENT EXAMINER